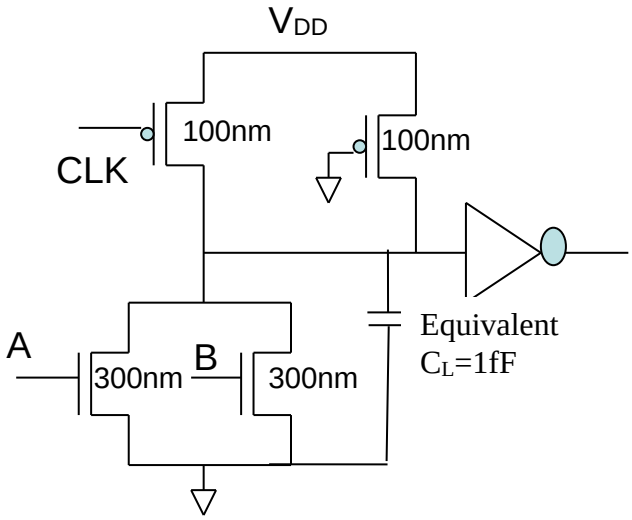
ECE 456
Mid-Term Examination 2
April 20, 2006

Name:_____
PUID:_____

1. Consider the dynamic gate shown below. Instead of a regular (conditional keeper), the circuit here shows a pseudo-NMOS keeper. The size of the keeper transistor is 100nm. The NMOS transistors are 300nm each in width. V_{DD} is 1V. Determine the speed of the logic gate . Assume that the inverter is ideal with a trip point at $V_{DD}/2$. (30 points)



	I_{ON} (/um)	**I_{OFF} (/um)**
NMOS	1nA	1mA
PMOS	0.4nA	250uA

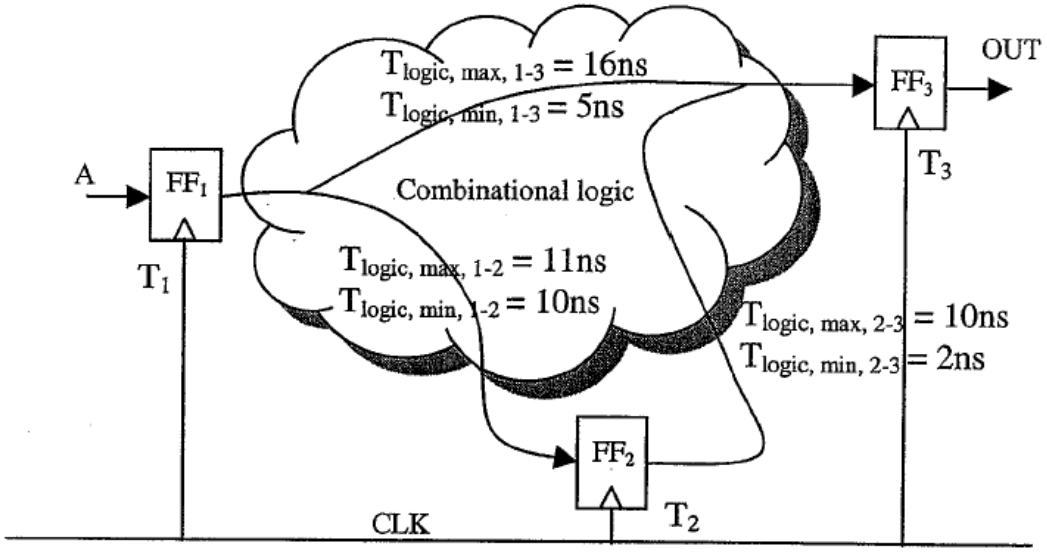
2. (a) Draw the circuit diagram of a clocked CMOS S-R Flip-Flop that can be used as an SRAM memory cell. (10 points)

(b)Indicate the modifications that you need to make so that it works as an SRAM cell. (5 points)

(c) Fill up the following table with appropriate voltage values. (5 points)

	During Read	**During write**
Word Line		
Bit Line		
$\overline{\text{Bit Line}}$		

3. Consider the following pipelined circuit



Consider that T_{C-Q} is 1ns, T_{setup} = 1.5ns and T_{hold} = 0.5ns
Find F_{MAX} and F_{MIN} for the circuit (25 points)

4. Consider a C^2 MOS latch based logic where the combinational logic, F is a NAND gate. One of the inputs of the NAND gate comes from a φ –latch and the other input is coming from an input pin. The output of the NAND gate goes to a φ/bar-latch. Draw the circuit diagram of the given logic.
Show how a 1-1 overlap can give rise to potential RACE conditions.
Propose a solution to this problem. (25 points)